With respect to the Office Action applicants also note that U.S. patent 5,925,926 to Watanabe cited in the rejection of claims 24 and 26 has not formally been made of record, i.e., that reference to Watanabe has not been properly listed on a PTO-892 form. Applicants request the proper listing of that reference on a PTO-892 form.

Addressing now the rejection of claims 21-23 and 25 under 35 U.S.C. § 112, first paragraph, that rejection is traversed by the present response.

Claims 21-23 and 25 were rejected as the specification was noted as not disclosing the partial covering of a Schottky diode with a covering of a diode region by an inner lead frame. In response to that rejection of claims 21-23 and 25 applicants traverse the position as applicants submit that the subject matter in claims 21-23 and 25 is fully supported by the original specification.

Applicants draw attention to Figure 8 and the original specification at page 17, lines 19-26. Those original disclosures show a mode in which the Schottky diode SBD is formed in the transistor chip Q2 as one unified structure. As noted in the specification at page 17, lines 19-26, the chip is applicable to the package shown in Figures 7A-7C. Further, as is clear for example in Figure 7A, since the inner lead 15_1 or 15_2 covers the greater part of transistor chip 9_1 or 9_2, it is clear to one of ordinary skill in the art that the inner lead covers at least a part, or the whole according to circumstances, of the Schottky diode SBD.

In such ways, one of ordinary skill in the art would clearly understand that the original specification supports the subject matter of claims 21-23 and 25, and therefore those claims are in full compliance with all requirements under 35 U.S.C. § 112, first paragraph.

Addressing now the rejection of claims 21-26 under 35 U.S.C. § 112, second paragraph, that rejection is traversed by the present response.

Each of independent claims 21 and 24 is amended by the present response to clarify that the Schottky diode is "connected in parallel to the transistor" of a transistor chip. Those

claim amendments are believed to address the rejection of claims 21-26 under 35 U.S.C. § 112, second paragraph.

Addressing now the rejection of claims 24 and 26 under 35 U.S.C. § 103(a) as unpatentable over Davis in view of Watanabe, that rejection is traversed by the present response.

Davis is directed to a MOSFET die and a Schottky diode die each mounted within a device package on a common lead frame pad with their drain and cathode terminals, respectively, connected together at the common pad.[1] In Davis the package lead is connected to the Schottky diode and the MOSFET by separate bonding wires, see for example Figure 3. Utilizing a connection with such separate bonding wires deteriorates heat radiation properties of the device.

In contrast to Davis, in independent claim 24 as currently written an inner lead frame made of sheet metal has the structure of "one end of the inner lead frame being connected to the main electrode on at least a part of the diode region, a second end of the inner lead frame being connected to a package lead". That is, in claim 24 as currently written the package lead is connected to both the Schottky diode and the MOSFET by one piece of sheet metal. Davis does not teach or suggest such a structure.

Further, Watanabe is only cited to disclose the use of inner leads made of sheet metal. Watanabe does not overcome the above-noted deficiencies of Davis as Watanabe also does not teach or suggest the use of one single piece of sheet metal to connect both a Schottky diode and the MOSFET.

Moreover, the structure set forth in claim 24 as currently written provides benefits that cannot be achieved in the applied art to Davis in view of Watanabe. Specifically, the structure in claim 24 as currently written provides an improved heat radiation property by

[1] See the Abstract of Davis.

connecting the package lead to both the Schottky diode and the MOSFET by sheet metal. Such a benefit is not taught, suggested, or even recognized in Davis or Watanabe.

Applicants also note that element 1 in Watanabe is an inner lead reinforcing pattern that mechanically fixes a chip and the TAB tape. Element 1 in Watanabe is in fact not even an inner lead frame for electrically connecting electrodes. Thus, even the relied upon teachings in Watanabe contradict with claims 24 and 26 as currently written.

In such ways, independent claim 24, and claim 26 dependent therefrom, distinguish over the combination of teachings of Davis in view of Watanabe.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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"RESPONSE UNDER 37 CFR 1.116-
EXPEDITED PROCEDURE EXAMINING
GROUP 2811 "

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IN THE CLAIMS

21. (Amended) A semiconductor device comprising:

a transistor chip having a first main electrode and a gate electrode for a transistor on an upper surface of the transistor chip, a second main electrode on a bottom surface of the transistor chip, and a Schottky diode [formed] connected [between the first and the second main electrode] in parallel to the transistor [chip];

a package base to which the second main electrode of the transistor chip is joined and connected;

an inner lead frame made of a sheet metal, one end of the inner lead frame being connected to the main electrode so as to cover at least a part of the Schottky diode, a second end of the inner lead frame being connected to a package lead.

24. (Amended) A semiconductor device comprising:

a transistor chip having a first main electrode and a gate electrode on an upper surface of the transistor chip, a second main electrode on an bottom surface of the transistor chip, a transistor region including a transistor, operation of which is controlled by the first main electrode, the gate electrode, and the second main electrode, and a diode region in which a Schottky diode is [formed] connected [between the first main electrode and the second main electrode] in parallel to the transistor;

a package base to which the second main electrode of the transistor chip is joined and connected;

an inner lead frame made of a sheet metal, one end of the inner lead frame being connected to the main electrode on at least a part of the diode region, a second end of the inner lead frame being connected to a package lead.